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Sixth Semester B.E. Degree Examination, Dec.2019/Jan.2020
Digital System Design using Verilog

Time: 3 hrs.

Max. Marks:100

**Note: Answer FIVE full questions, selecting
atleast TWO questions from each part.**

PART – A

- 1 a. What is meant by design methodology? Enlist the basic steps of design methodology with help of a flowchart. (12 Marks)
- b. Explain the concept of real world circuit for,
 - i) Static load levels ii) capacitive and propagation delay. (08 Marks)
- 2 a. Why it is better to use a low level logic level rather than a high logic level? Explain. (04 Marks)
- b. What is bit flip? How to deal with invalid code in the design. (06 Marks)
- c. Develop a verilog model for a 7-segment decoder that includes an additional input, "BLANK", that overrides the BCD input and causes all segment not to lit. (10 Marks)
- 3 a. Explain and implement a 4-bit carry look ahead adder circuit. (06 Marks)
- b. Develop a verilog model of an adder/subtractor for 12-bit unsigned binary numbers. The circuit has data inputs x and y, a data output s, a input mode that is 0 for addition and 1 for subtraction, and an output ovf_unf that is 1 when an addition overflow or a subtraction underflow occurs. (06 Marks)
- c. Prove that negating a signed integer X is nothing but 2's compliment of X. (05 Marks)
- d. What number is represented by the fixed-point binary number 01100010, assuming the binary point is four places from the right? (03 Marks)
- 4 a. Design and develop circuit and code for decode counter. (05 Marks)
- b. Develop a verilog model of a de-bouncer for a push button switch that uses a de-bounce interval of 10ms. Assume the system clock frequency is 50MHz. (10 Marks)
- c. Explain about sequential datapath and control in digital design. (05 Marks)

PART – B

- 5 a. Explain different memory types. (10 Marks)
- b. Write about : i) parogrammable array logic ii) FPGAs. (10 Marks)
- 6 a. Explain the elements of embedded computer with a neat diagram. (10 Marks)
- b. Briefly explain the interfacing with memory with an example. (10 Marks)
- 7 a. Write a short note on :
 - i) Multiplexed bases (10 Marks)
 - ii) Open drain bases.
- b. Explain the serial transmission technique. Also explain the three basic ways in which we can synchronize the transmitter and receiver. (10 Marks)
- 8 a. With a neat diagram and flow chart explain the design flow including hardware/software design. (10 Marks)
- b. Write a note on design optimization. (10 Marks)

Important Note : 1. On completing your answers, compulsorily draw diagonal cross lines on the remaining blank pages.
2. Any revealing of identification, appeal to evaluator and /or equations written eg, 42+8 = 50, will be treated as malpractice.